CLAIMS

1. A circuit comprising:

a reference signal;

a frequency synthesizer, receiving a dithered signal and the reference signal, generating a constant frequency output; and

configuration registers transceiving data and control signals with the frequency synthesizer.

2. A circuit, as defined in claim 1, further comprising a modulated analog phase lock loop, receiving the reference signal, generating the dithered signal.

3. A circuit, as defined in claim 1, the frequency synthesizer comprising:

a predictor and corrector that receive the dithered signal and the reference signal, generating a "remove pulse" signal; and

an output generator, receiving the dithered signal, reference signal, and "remove pulse" signal, generating a "clear pulse" signal and the constant frequency output.

4. A circuit, as defined in claim 1, the frequency synthesizer comprising:

a predictor, generating a first output signal indicative of the average number of dithered periods to remove per dithered period;

a corrector receiving the first output signal, generating a second output signal indicative of the fractional number of dithered periods to remove each dithered period; and

an accumulator receiving the second output signal, operative to count the fractional number of dithered periods, removing a dithered period when an integer has been reached.

5. A circuit, as defined in claim 4, the predictor comprising:

means for measuring the average number of dithered periods for the sample of the reference signal;

a comparator, receiving the first output signal and a desired number of dithereds periods per sample of the reference signal, generating a difference indicative of the average number of dithered periods to remove per sample of the reference signal; and

a multiplier, receiving the difference, operative to scale the difference according to a scale factor register value.

6. A circuit, as defined in claim 4, the corrector comprising:

means for measuring error from the last sample;

means for determining a scale to fractional error; and

an adder, receiving the scale to fractional error and the average number of dithered periods to remove per dithered period, generating the difference.

7. A circuit, as defined in claim 1, the frequency synthesizer including:

a first synchronizer, receiving the system clock as reference input and the PLL output, generating a first output;

an edge detector, receiving the first output and the PLL output, generating an edge signal;

a second synchronizer, receives an enable signal and the system clock, generating a second output;

an adder, receiving reference count signals, generating adder output signals;

an Expected Count Latch, receiving the second output as a clear input, the system clock as a clock input, the adder output signals as data, and the edge signal as a load signal, generating a latch output;

wherein the adder further receives the latch output;

an Edge Counter, receiving the system clock and the second output as a clear signal, generating a counter output;

a comparator, receiving the counter output and the latch output, generating a rollover output, an A>B+1 signal, and an A>B signal.

8. A method for frequency synthesis comprising:

receiving a dithered signal and a reference signal;

selecting a desired number of periods in the dithered signal to receive during a sample period of the reference signal;

counting the actual number of periods in the dithered signal during the sample period;

comparing the desired number to the actual number;

generating a constant frequency signal based on the comparison.

9. A method for frequency synthesis comprising:

receiving a dithered signal and a reference signal;

determining an average fractional number of dithered periods of the dithered signal to remove each dithered period;

determining a fractional error of dithered periods for each dithered period based on a period of the reference signal; and

combining the average fractional number and the fractional error generating a fractional number of dithered periods to remove each dithered period; and

generating a constant frequency signal based on the combination.

10. A method for frequency synthesis, as claimed in 9, determining an average fractional number of dithered periods comprising:

measuring an average number of dithered periods for a sample of the reference signal;

generating a difference from the average number of dithered periods and a desired number of dithered periods per sample of the reference signal, the difference indicative of the average number of dithered periods to remove per sample of the reference signal; and

scaling the difference according to a scale factor register value.

11. A method for frequency synthesis, as defined in claim 9, determining a fractional error of dithered periods for each dithered period comprising:

measuring error in a number of dithered periods corresponding to a given sample of the reference signal;

determining a scale to fractional error; and

scaling the scale to fractional error to generate the fractional error.

12. A method for frequency synthesis, as defined in claim 11, wherein determining a scale to fractional error comprises referring to a look-up table.

13. An apparatus for frequency synthesis comprising:

a predictor operative to estimate an average amount of correction per sample;

a corrector operative to measure actual error in a previous sample;

an accumulator, connected to the predictor and corrector, generating an accumulator output signal indicative of the sum of the average amount of correction and the actural error;

an output generator, receiving the accumulator output signal, generating an output signal having constant frequency.